# Single-Event Upset in Commercial Silicon-on-Insulator PowerPC Microprocessors

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***Abstract* –Single-event upset effects from heavy ions and protons are measured for Motorola and IBM silicon-on-insulator (SOI) microprocessors, and compared with results for similar devices with bulk substrates. The cross sections of the SOI processors are lower than their bulk counterparts, but the threshold is about the same, even though the charge collections depth is more than an order of magnitude smaller in the SOI devices. The upset rates are low enough to allow these devices to be used in space applications where occasional register or functional operating errors can be tolerated.**

## I. Introduction

Single-event effects can be a significant problem for devices operating in space, particularly for microprocessors because of their complexity. Radiation tests are often required in order to allow estimates of upset rates caused by space radiation. The test results help to determine what kinds of effects are produced and how they can be detected and overcome. Complex failure modes are of particular interest because they potentially limit ways in which errors and malfunctions can be detected and corrected by hardware or software techniques.

In recent years there has been increased interest in the possible use of unhardened commercial microprocessors in space because they operate at higher speed, and have superior electrical performance compared to hardened processors. However, unhardened devices are susceptible to upset and degradation from radiation, and more information is needed on how they respond to radiation before they can be used in space. Only a limited number of advanced microprocessors have been subjected to radiation tests, and the majority have been older device types which are designed with much larger feature sizes and higher operating voltages than modern devices [1-6].

High-performance CMOS devices are usually fabricated on epitaxial substrates with depth of about 2 $\mu$m between the epi-layer and highly doped substrate [7]. Partially depleted silicon-on-insulator processes use tub depth between 0.15 and 0.18 $\mu$m [8], reducing the charge collection depth for normally incident ions by more than an order of magnitude compared to similar processes with conventional isolation (on thin expitaxial substrates). Because of the much smaller charge collection depth, the single-event upset (SEU) sensitivity of SOI devices is expected to be much better. However, other factors, such as lower operating voltages, reduced junction capacitance and amplification by parasitic bipolar transistors [9] may limit the degree of improvement in SEU sensitivity that can be obtained with commercial SOI processors. This paper examines SEU effects in advanced SOI processors from two manufacturers, comparing the results with advanced processors that use conventional isolation methods from each manufacturer.

## II. Device Descriptions

The PowerPC 750 was co-designed by IBM and Motorola. It is a 64-bit processor that has evolved into improved versions (with different numerical designations) during the last five years, taking advantage of manufacturing improvements that have allowed the feature size and internal operating voltage to be reduced, as well as an increase in the overall functionality. We previously reported SEU measurements on earlier generation PowerPC 750 microprocessors from both manufacturers [1].

Commercial manufacturers have shown interest in using SOI technology for fabricating low-power, high-performance microprocessors. The Motorola PowerPC 7455 and IBM PowerPC 750FX are the latest generation of the PowerPC family which are fabricated with SOI technology. They are partially depleted with no body ties. The thickness of the active Si layer for the Motorola part is 110 nm. The IBM part has a thickness of 117 nm. The Motorola PowerPC 74xx series (G4 family) incorporates a more advanced processing unit (AltiVec). The AltiVec unit can perform four single precision floating point or sixteen byte calculations, in a single cycle.

Table 1 shows how the recent SOI generation of the PowerPC family fits with previous bulk generations of the PowerPC family. The feature size of the SOI Motorola PowerPC is reduced from 0.29 to 0.18 $\mu$m, with the core voltage reduced from 2.5 to 1.6 V. The feature size of the SOI IBM PowerPC is reduced from 0.22 to 0.13 $\mu$m, with the core voltage reduced from 2.0 to 1.4 V. The larger die size of the SOI PowerPC's are due to the more advanced design.

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This paper reports test results for the Motorola SOI PowerPC 7455 and IBM SOI PowerPC 750FX, as well as results for the Motorola PowerPC 7400 (G4), which is fabricated with standard isolation (epitaxial layer on heavily doped substrate). The radiation tests examined upsets in the registers, the L1 data cache and their tags, L2 tags, and the Translation Lookaside Buffer (TLB of the Memory Management Unit, MMU), as well as overall results for processor functionality. Tests were done using energetic protons and heavy-ion beams. The protons have sufficient range to penetrate the packaging material of the PowerPC, but heavy-ion beams that were available have limited range and cannot penetrate the package. In order to overcome this limitation, tests were done on specially prepared units that were thinned so that irradiation from the back of the die penetrated to the front side of the die.

Table 1. Summary of Motorola's and IBM's PowerPC Family of Advanced Processors.

| Device | Feature Size ($\mu$ m) | Die Size ($mm^2$) | Core Voltage (V) | Maximum Operating Frequency (MHz) |
|---|---|---|---|---|
| Motorola MPC750 (G3) | 0.29 | 67 | 2.5 | 266 |
| Motorola MPC7400 (G4) | 0.20 | 83 | 1.8 | 400 |
| Motorola MPC7455 (SOI) | 0.18 | 106 | 1.6 | 600 |
| IBM PPC750 | 0.22 | 40 | 2.0 | 307 |
| IBM 750FX (SOI) | 0.13 | 34 | 1.4 | 800 |

## III. Experimental Method

Radiation testing of the Motorola SOI processor was done using a development board from Motorola known as "Sandpoint". Radiation testing of the IBM SOI processor was done using a development board from Motorola known as "Yellowknife". These boards were chosen because they eliminated the large engineering effort that would be required to design a custom test board for the processor. They also provided a basic PROM-based system monitor instead of a complex operating system. This provides far better diagnostic information and control of processor information during SEU testing compared to more advanced operating systems. These boards have a daughter card for the processor with no active components underneath, which is important for proton tests, where high energy protons could strike other components on the test board. This allowed us to shield other components on the board during proton tests, assuring that the measured response was entirely due to effects within the processor. The only external communication channels provided on these boards are a simple serial connection for a "dump" terminal and a JTAG port. An Agilent Technology 5900B JTAG probe was used for our tests. This probe made it possible to interrogate the processor even after unexpected events occurred (such as operational errors during irradiation). The methodologies used in these tests are briefly described below. Detailed descriptions of them can be found in [1] and earlier work by Koga et al. [10].

A number of assembly language software programs were written to detect errors in various sections of the processor. It was possible to design software that primarily exercised specific registers or regions, and thus allowed the number of errors to be determined for various registers or for specific operating modes. During some of the tests, the processor became non-functional (program "hangs" or SEFIs - Single Event Functional Interrupts), and these types of errors are of extreme concern in applications because they may require complex procedures to restore normal operation. In most cases it was not possible to determine the underlying cause of these malfunctions because there are many possible ways in which processor operation can be disrupted. However, the relative occurrence of "hangs" was measured and compared to the upset rate obtained for internal registers or other functions of the processor.

Minimizing processor activity during irradiation essentially reduces the number of internal operations, thereby making the operation susceptible to errors in only a few internal locations. In our test method, "do nothing with strip chart", the processor was programmed to perform a one word instruction in a small infinite loop and write a register snapshot to a strip chart in the physical memory every half second. After the irradiation ended, an external interrupt triggers a program to count state changes in internal registers or the data cache.

A more complex method was required to examine errors in the L1 cache. Upsets in the cache were counted with special post beam software. The cache was initialized under specified conditions prior to irradiation and then disabled. Then a clearly recognizable pattern, designed to be distinctly different from contents of the cache, was placed in the external memory space covered by the cache. Comparing the cache contents after irradiation provided verification of the cache contents. Tag upsets, as well as upsets of the data valid flag, were detected by monitoring the distinctly different pattern. The tag and data valid upsets were thus distinguished and counted separately from upsets of the data bits themselves.

There is no instruction that directly accesses the contents of the TLB. Therefore, we applied the following methodology to measure upsets in the TLB. Prior to irradiation, the memory was divided into two separate data groups. Each data group was filled with its own physical address. The two Page Table Entry Groups were set in two different locations of memory. The first Page Table Entry Group mapped to the first section of the filled area. The second Page Table Entry Group mapped to the second data group of memory. Then the Memory Management Unit was enabled, and memory was mapped using the first Page Table Entry Group. This method caused TLB's to be filled by the first Page Entry Group. The Memory Management Unit was disabled and an infinite loop was executed during the irradiation. After the irradiation had ended, an external interrupt exited the loop and enabled the Memory Management Unit with pointers to the second Page Table Entry Group. The Memory Management Unit checked the TLB's to obtain a valid Page Table Entry. In case there was an upset and no valid entry,

the Memory Management Unit commenced to obtain a valid Page Table Entry from the second Page Table Entry Group. Data was read from the first group and compared with their addresses. Differences indicate at least one upset bit the corresponding Page Table Entry in the cached TLB.

Proton tests were performed at the University California Davis cyclotron. Because of sufficient range of protons to penetrate the packaging material of the SOI PowerPC's, tests were done in the air.

Heavy-ion tests were performed at the Texas A&M accelerator. All irradiations were done using ions with normal incidence. This facility produces the long-range ions needed for SEU testing through thick materials. Particularly, the 25 and 40 MeV/amu beams are quite penetrating, and it is possible to do irradiations in the air rather than in vacuum. Undegraded Ion beam used in our measurements were listed in Table 2.

Table 2. List of the ion beams used in our measurements (Range and LET are in Si).

| Ion | Energy per Nucleon **MeV/amu** | LET **MeV-cm$^2$ /mg** | Range **$\mu$ m** |
|---|---|---|---|
| Ne | 40 | 1.2 | 1648 |
| Ar | 40 | 3.8 | 1070 |
| Kr | 40 | 14.2 | 601 |
| Ne | 25 | 1.7 | 790 |
| Ar | 25 | 5.4 | 491 |

The total thickness of the die for SOI PowerPC's is about 850 $\mu$m and the limited range of heavy-ion beams does not allow them to penetrate the package, except for ions with lower LET. The "flip-chip" design of the SOI PowerPC's does not allow the device to be "delidded" without destroying pad and bonding connections. In order to get around the delidding problem, the back surface of the PowerPC's was ground with a precision high-speed diamond grinding machine This reduced the total thickness of the die for the Motorola processor from about 850 to 230 $\mu$m, which is thin enough to allow adequate penetration of the die using back irradiation with the high-energy ions available at the accelerator. The thinning process did not change any observed electrical parameters of the processor. The IBM processor was tested without thinning. This limits useable ions (see table 2) to those with a range greater than 850 $\mu$m , i.e. only the 40 MeV/amu Ne and Ar. Thus, the highest LET is limited to about 18.8 MeV-cm$^2$ /mg. Corrections to the LET were made to account for energy loss of the ions when they traverse the back layer to the thin epitaxial region at the surface. This approach was used in earlier tests of the PowerPC 750, and there was good agreement for SEU results obtained from thin and unthinned PowerPC processors, after correcting for energy loss through the thinned substrate [1].

Heating is always an issue for high-speed processors. A custom heat sink with a hole for the processor die was used to conduct heat away from the package. A thermocouple was used to measure temperature during the time that the device operated. Also, a routine was developed to read out the processor's junction temperature. In addition a fan was used to cool the heat sink and JTAG probe.

## IV. Test Results

### A. *Heavy-Ion Tests- Normal Processor Operation*

Basic Procedure

The methods discussed in the previous section were used to measure the single-event upset rates for Registers, Data-Cache Memory, Data Cache Tags and Flags, Instruction Cache Memory and TLB. The measurements for registers included General Purpose Registers (GPR), Floating Point Registers (FPR), Special Purpose Registers (SPR) and AltiVec Registers for Motorola SOI PowerPCs. These measurements were done for LET ranges between 1.36 and 25.2 MeV-cm$^2$ /mg. For the IBM SOI processor we measured SEU for Registers, Data-Cache Memory, and Data-Cache Tags and Flags. These measurements were done for LET ranges between 1.7 and 19 MeV-cm$^2$ /mg using irradiation from the back on thinned samples.

Motorola Processors

Figure 1 displays results of cross section measurements for the Motorola SOI PowerPC D-Cache for "0" to "1" transitions along with results for the two bulk processors. Even though the G4 processor has a much smaller feature size than the PowerPC 750 (as well as lower core voltage), the threshold LET is likely not very different. The cross section of the G4 is slightly lower, which is consistent with the reduced cell area. These results suggest that scaling between 0.3 and 0.2 $\mu$m feature size has little effect on SEU sensitivity. However, this trend may not continue as devices and core voltages are changed to even lower values.

The LET threshold of the SOI processor is about 1 MeV-cm$^2$ /mg, and appears to be slightly lower than the LET threshold of the bulk processors. That result is somewhat surprising. The saturation cross section of the SOI is more than an order of magnitude lower than that of the bulk processors. These differences between the bulk and SOI processors will be discussed further in Section V.

The large number of storage locations within the data cache allows more statistically significant numbers of errors to be measured, decreasing the error bars due to counting statistics. The error bars are ~2 sigma and result from Poisson statistics. For the data points where statistical error bars are not shown, they are smaller than the size of the plotting symbols. The cross section for "1" to "0" transitions was the same as that for for "0" to "1" transitions. These data were taken with thin and normal ("unthinned") processors. The LET at the device surface was corrected to allow for decrease in beam energy as ions traversed the device from back to the sensitive top surface of the device. There was good agreement for results obtained from different thicknesses.

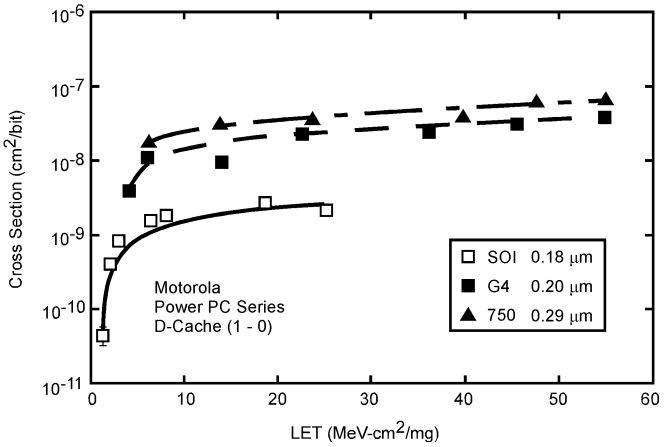


Figure 1. Comparison of the heavy-ion single-event-upset cross-section for the data cache bits transitions from "0" to "1" of the Motorola SOI PowerPC to those of the PowerPC 750 and G4.

Figure 2 shows results of heavy-ion measurements for the TLB of the Motorola SOI PowerPC MMU, as well as for the two bulk processors from Motorola. The LET threshold of the various processors was nearly the same, regardless of technology or feature size. The saturated cross section of the SOI processor is about $4 \times 10^{-9}$ $cm^2$/bit, about 1/10 that of the equivalent bulk PowerPCs. These results are similar to those observed for D-Cache Memory (Figure 1).

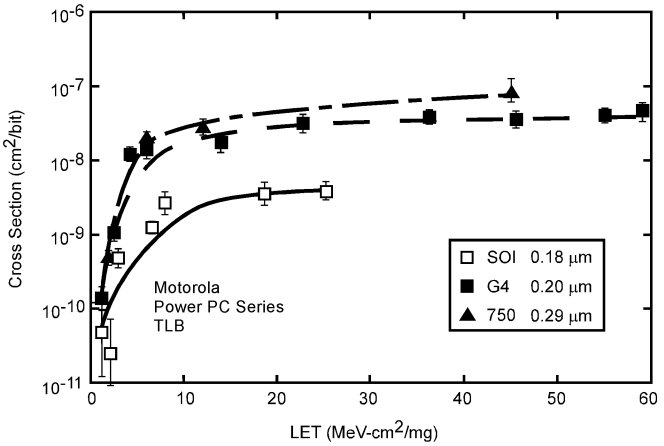


Figure 2. Comparison of the heavy-ion single-event-upset cross-section for the TLBs of the SOI PowerPC to those of the PowerPC 750 and G4.

Figure 3 shows results of heavy-ion cross section measurements for Floating Point Registers for "0" to "1" transitions. The ions used in tests of the bulk processors did not have sufficiently low LET to determine the threshold, but a more complete series of tests was done for the SOI processor that show the onset of upsets at LET values below 1 MeV-$cm^2$/mg. The saturated cross section of the SOI processor is about $1 \times 10^{-8}$ $cm^2$/bit, about a factor of four higher than the saturation cross section of the data cache (Figure 1). The cross section for "1" to "0" transitions was more than an order of magnitude lower for the SOI device. There is no Single Event Upset below an LET of 18.8. The measured cross section at an LET of 25.2 MeV-$cm^2$/mg is $1.14 \times 10^{-9} \pm 7.7 \times 10^{-10}$. This is contrary to the results for the Motorola PowerPC 750 and G4. For those processors the cross section for "1" to "0" transitions was statistically the same as for "0" to "1" transitions [1].

IBM Processors

We were unsuccessful in getting a working version of a thinned IBM SOI processor (very few units were available). Therefore, all of the heavy ion tests were done on standard devices with a substrate thickness of about 850 $\mu$m. This restricted the maximum LET to about 19 MeV-$cm^2$/mg.

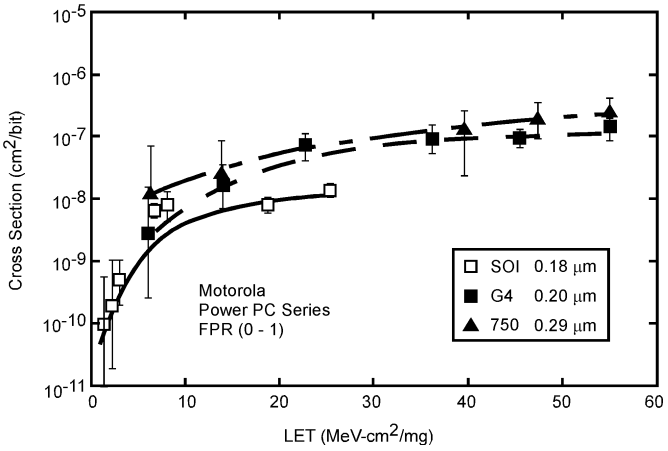


Figure 3. Comparison of the heavy-ion single-event-upset cross-section for the Floating Point Registers (FPR) of the Motorola SOI PowerPC to those of the PowerPC 750 and G4.

Figure 4 displays results of cross section measurements for the IBM SOI PowerPC D-Cache for "1" to "0" transitions, along with older results for the IBM PowerPC 750. The LET threshold appears to be below 1 MeV-$cm^2$/mg, and is very similar to the threshold LET observed for the SOI processor from Motorola. Note that the IBM processor has a smaller feature size and lower core voltage. The saturated cross section is about $2 \times 10^{-9}$ $cm^2$/bit, the same as for the Motorola part. The cross section for "0" to "1" transitions was the same as that for "1" to "0" transitions. The saturated cross section for IBM SOI PowerPC is lower than that of the bulk device by a about a factor of 10, just as for the Motorola devices.

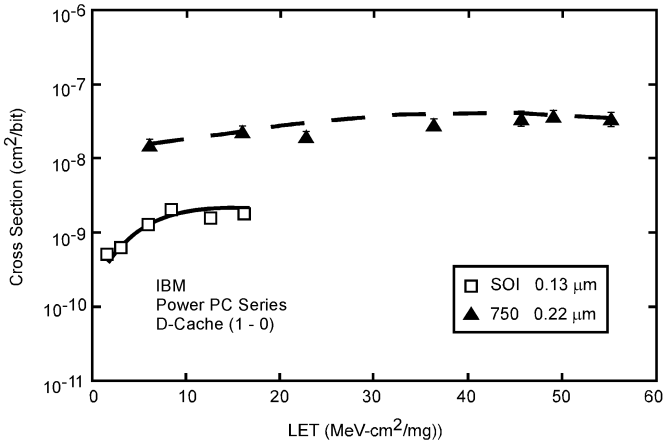


Figure 4. Comparison of the heavy-ion single-event-upset cross-section for the data cache bits transitions from "1" to "0" of the IBM SOI PowerPC to those of the PowerPC 750.

In Figure 5 we show results of cross section measurements for the IBM SOI PowerPC Floating Point Register (FPR) for "1" to "0" transitions. The saturated cross section is about $7x10^{-9}$ $cm^2$/bit. In contrast to the results for the IBM PowerPC 750 the cross section for "1" to "0" transitions was not the same as the cross section for "0" to "1" transitions (as discussed earlier, that same asymmetry was also observed for the Motorola SOI processor, but the "0" to "1" cross section was higher). For the IBM SOI device, the "0" to "1" cross section was about a factor of 8 lower than for "1" to "0" transitions. There is no Single Event Upset below an LET of 18.8. The measured Cross section at an LET of 18.8 MeV-$cm^2$/mg is $4.56x10^{-10} \pm 2.5x10^{-11}$.

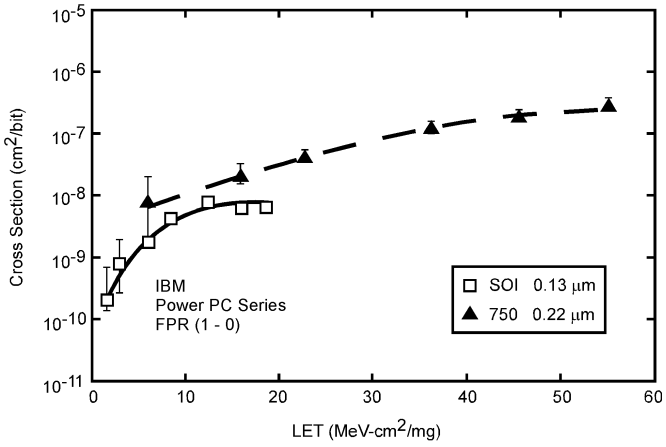


Figure 5. Comparison of the heavy-ion single-event-upset cross-section for the Floating Point Registers (FPR) of the IBM SOI PowerPC to those of the PowerPC 750.

### *B. Functional Errors ("Hangs")*

We also examined complex functional errors ("hangs") where the processor operation is severely disrupted during irradiation. We detected hangs by applying an external interrupt after the irradiation was ended; if the processor responded to the interrupt, then the processor was still operational to the point where normal software means could likely restore operation. If the interrupt could not restore operation, then the status was categorized as a "hang." In nearly all cases, it was necessary to temporarily remove power from the device in order to recover, and reboot the device.

In order to roughly scope problems with hangs, we calculated the hang cross section defined as the number of times the processor would not respond to the external interrupts divided by the total fluence to which the processor had been exposed. This was done for each LET. Figure 6 shows estimated cross section for hangs during heavy-ion measurements. The threshold LET appears comparable to that obtained for register errors. The cross section per device due to "hangs" is about $10^{-6}$ $cm^2$ for LETs above 4 MeV-$cm^2$/mg. For comparison we also display results for the Motorola G4. The saturated cross section for the SOI PowerPC is lower by a factor of 10 compare to G4 results. From an application standpoint, program "hangs" can be severe problems even if they occur infrequently because of the difficulty of identifying the malfunction and determining how to restore operation afterwards.

A less complete data set was available for the IBM SOI processor, which did not allow us to quantify the cross section for "hangs".

Although the threshold LET for "hangs" is low, the cross section is small enough so that the expected incidence of "hangs" is not very high in typical space environments. For example, the probability of "hangs" from galactic cosmic rays is about one in 25 years for the Motorola SOI processor.

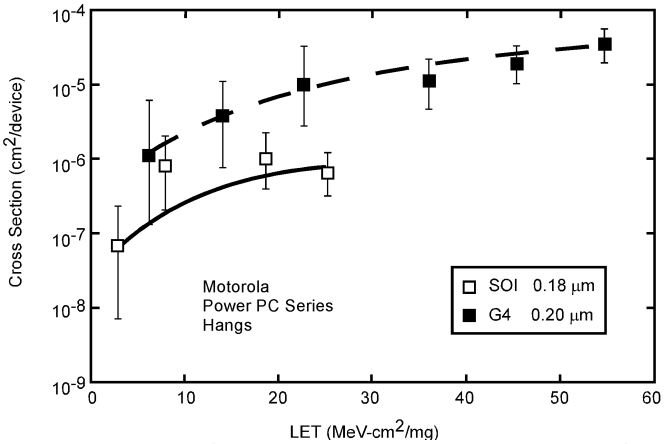


Figure 6. Comparison of the heavy-ion single-event-upset cross-section for the hangs of the Motorola SOI PowerPC and G4.

### *C. Proton Tests*

Motorola Processors

For the Motorola SOI processor we measured the single-event upset rates for the AltiVec Registers, Data-Cache Memory, Instruction-Cache Memory, Data-Cache Tags and Flags, and the TLB. These measurements were done for proton energies between 20 and 63 MeV, using thinned devices for energies below 50 MeV. Corrections were

applied to account for energy loss within the device at low energies.

Figure 7 shows results of cross section per bit measurements for TLB of the Motorola SOI PowerPC MMU versus proton energy (results for register tests were comparable). We also show previous measurements for the Motorola PowerPC 750 [1] and new results for the G4. The saturated cross section for the SOI processor is about $1x10^{-14}$ $cm^2$/bit, about a factor of five lower than the cross section for the bulk processors. The threshold energy is less than 20 MeV.

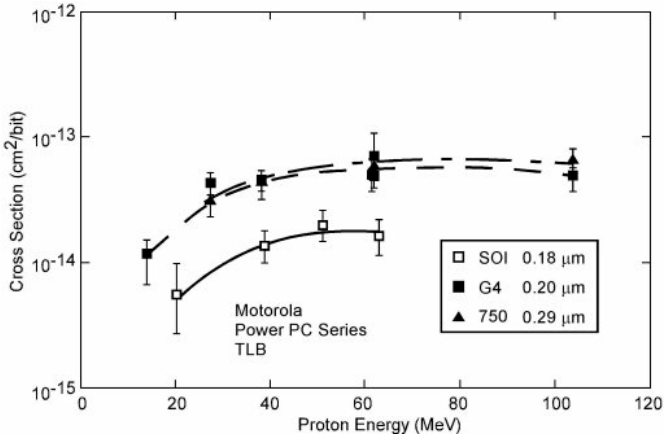


Figure 7. Comparison of the proton single-event-upset cross-section for the TLBs of the Motorola SOI PowerPC to those of the PowerPC 750 and G4.

IBM Processors

For IBM SOI processor we measured the single-event upset for the Registers, Data-Cache Memory, Data-Cache Tags and Flags. Figure 8 shows results of cross section measurements for the IBM SOI Data-Cache Memory bits for "1" to "0" transitions. The cross section for transitions between "1" and "0" were statistically identical for the SOI processor. Because tests of the SOI part were done on unthinned devices, there is some uncertainty in the cross section at the lowest energies. The older results for the PowerPC 750 were done with thinned samples.

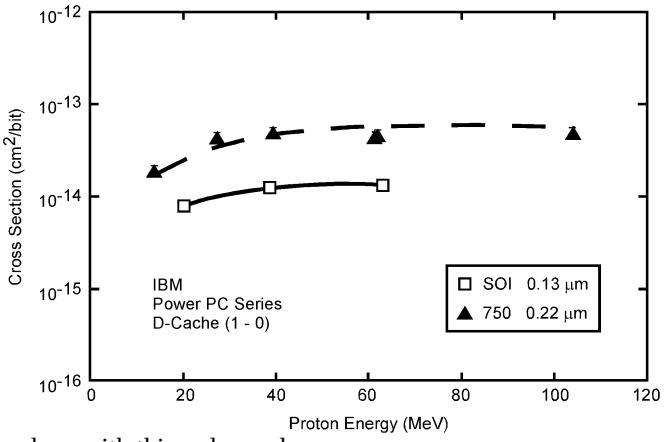


Figure 8. Comparison of the proton single-event-upset cross-section for the data cache bits transitions from "1" to "0" of the IBM SOI PowerPC to those of the IBM PowerPC 750.

The saturated cross section is about $1x10^{-14}$ $cm^2$/bit, which is lower compare to the data for the IBM PowerPC750 with its feature size of 0.22 $\mu$m [1]. This indicates that the higher density and increased speed of the SOI PowerPC does not increase the sensitivity of the registers to upset from protons. The threshold energy is less than 20 MeV for the SOI device. Future work will be done using thinned devices to provide better estimate for the threshold energy.

## V. Discussion

### A. Effects of Scaling on Junction-Isolated CMOS

Scaling for high-performance technologies depends heavily on reducing feature size, but also requires a reduction in power supply voltage [11]. Considerable work has been done showing that the critical charge for scaled devices is expected to be lower for more advanced devices [12]. This often leads to the conclusion that single-event upset will be far more severe for highly scaled devices. However, this has not been observed for high-performance devices such as microprocessors [13]. Other factors cause less charge to be collected as devices are scaled to smaller feature size.

Although changes in the underlying epitaxial layer thickness helped reduce collected charge in older processors, epitaxial layer thicknesses have not changed very much in recent years, and are typically between 2 and 2.5 $\mu$m. Thus, although doping levels in the channel region increase with scaling, the charge collection depth is not expected to change significantly for the bulk/epi processors in the present study.

However, charge collection will be lower when feature sizes are reduced below about 0.25 $\mu$m because the lateral distribution of charge from the ion track will extend beyond the active area. Charge collection efficiency has been investigated by Shin for alpha particle upset in CMOS devices below 1 $\mu$m [14]. Computer modeling was used to show that charge collected from an alpha particle was reduced by about 25% for a 0.3 $\mu$m trench isolated process compared to the charge collected in an equivalent process with a feature size of 0.8 $\mu$m. The decreased junction area and lower voltage (required from scaling laws) both contributed to the reduced charge collection. This suggests that charge collection efficiency may be one of the reasons that the overall SEU sensitivity of advanced processor is only slightly affected by scaling. The decrease in critical charge is compensated by smaller area along with decrease charge collection efficiency.

Although it is useful and instructive to make comparisons of single-event upset results as microprocessors within a given family evolve, one must remember that these are complex devices, not test structures. Other factors in the processor design may also affect the way that different processors in the series respond to radiation. There are also different requirements for various registers and functions within the device. For example, access time is a critical requirement for on-board cache, but cache single-event upset results may not be representative of other types of registers within the device.

The results for the Motorola G4 processor in this paper show lower cross section and slight increases in threshold LET compared to the PowerPC 750, even though the core voltage for the G4 was reduced from 2.5 to 1.8 V, and the feature size from 0.29 to 0.20 $\mu$m. The cross section per bit was about 30% lower for the cache in the advanced G4, and a similar reduction in cross section was observed for the floating-point registers at high LET. Proton cross sections were nearly identical for the G4 and the older PowerPC 750. These results suggest that advanced bulk processors have sufficiently low rates to allow their use in space, providing that software techniques are implemented that can correct for errors in registers, cache, and other registers within the device. However, internal operating margins will decrease as manufacturers continue to reduce core voltage and increase clock speed, and device complexity will also increase. Thus it will likely be necessary to evaluate new processors or older processor types that have migrated to more advanced processors in order to assure that upset rates and complex failure modes are still within acceptable limits, even though scaling efforts to date have not had much impact on SEU sensitivity for bulk/epi processes.

*B. Silicon-on-Insulator Upset Effects*

The effect of scaling on partially depleted SOI structures is a far more difficult problem. The main advantage of SOI is marked reduction in the thickness of the silicon region for charge collection. To first order, this should decrease the collected charge by more than an order of magnitude compared to bulk/epi devices with equivalent feature size, increasing the threshold LET by at least a factor of ten. However, charge amplification from the parasitic bipolar transistor that is inherent in partially depleted SOI increases the charge by a significant factor. Although the charge amplification effect can be reduced by adding body ties to the structure, neither of the two SOI processors in our studies used body ties. That mechanism has been studied by several researchers, including Musseau, [15] and more recent work in the electron device community [14,16].

Work by Hirano, et al. on SOI SRAMs with a feature size of 0.18 µm showed more than two orders of magnitude reduction in soft error rates for SOI devices compared to bulk processes with the same feature size and trench isolation [17]. They also ran computer simulations showing that the drain current from alpha particles was extended in time by about two orders of magnitude for SOI structures without body ties, where the bipolar effect becomes important. They ran the simulations for two voltage conditions: 1.0 and 1.8 V. Their results suggest that the advantage of SOI for SEU is negated unless body ties are used in the design.

Dodd, et al. studied charge collection in SOI structures with a film thickness of 250 nm and power supply voltage of 3.3 V [18]. Their experiments, using focused ion beams, showed excess charge collection. They postulated that this was due to charge collection from the extended substrate, *through the buried oxide*. That work showed that charge collection in SOI devices is a highly complex problem, requiring further work in order to realize the potential hardening advantages of SOI structures for single-event upset. The substrate charge collection mechanism that they observed has not been reported in work done by the electron device community, which concentrates on upset effects from alpha particles and atmospheric neutrons, but workers in the device community have not considered the possibility of charge collection beyond the confines of the buried oxide.

Silicon film thickness is a critical factor in SOI single-event upset. From the standpoint of electrical device design, there is a tradeoff between bipolar gain and the history effect (which causes switching waveforms to depend on previous switching waveforms). The history effect can be reduced by decreasing film thickness, but that increases bipolar gain. IBM has determined that a film thickness of 117 nm is an optimum design point [19,20]. The film thickness of the Motorola processor was found to be 110 nm. Thus, the film thicknesses of the two SOI processors in the present study are very similar. However, the feature size of the IBM device is much smaller – 0.13 $\mu$m - compared to the 0.18 µm feature size of the Motorola device. Thus, it is somewhat surprising that the single-event upset results for the two SOI processors are so similar, given the difference in feature size and core voltage. Figure 9 displays the comparison of D-cache measurements for the Motorola and IBM SOI PowerPC's.

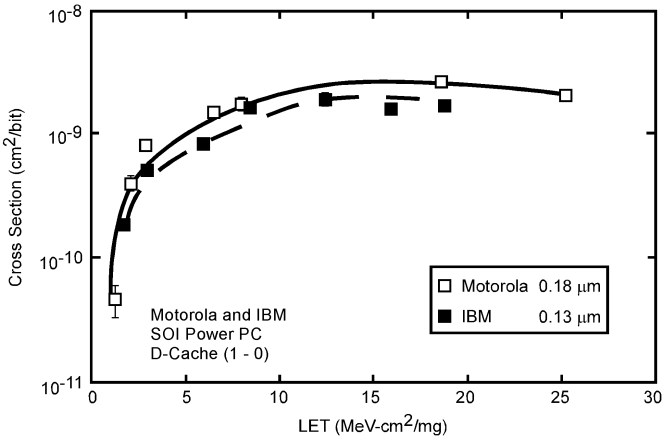


Figure 9. Comparison of the Heavy ion single-event-upset cross-section for the data cache bits transitions from "1" to "0" of the Motorola SOI PowerPC to those of the IBM SOI PowerPC.

*C. Upset and Cross Section for SOI Devices*

It is also of interest to compare our results with older results (1997) by Brothers, et al. [21] on SOI SRAMs that were fabricated by IBM with a feature size of 0.25 $\mu$m. They did not test their devices at LET values below 10 MeV-cm$^2$/mg, and consequently they could only estimate the threshold LET. However, they made direct comparisons between a bulk/epi version of the SRAM with the SOI version. Within the limits of their measurements, they determined that the threshold LET of the bulk/epi and SOI memories were the same, which is similar to the results in the present paper for microprocessors. The saturation cross section of the SOI memory in the work by Ref. 20 was also an order of magnitude lower than that of the bulk/epi device. They reported a sensitive area of about 1.5

$\mu$ m$^2$/bit at high LETs. Dodd, et al. [18] noted that this cross section is probably too high unless charge from the drain (or other regions, such as the substrate conduction mechanism) add to charge collected beneath the gate region.

We measured much smaller cross sections – about 0.15 $\mu$ m$^2$ /bit – for the data cache in the Motorola SOI processor, which has a feature size of 0.18 $\mu$m. The cross section for TLBs and floating point registers was about a factor of 2.5 higher, implying that excess charge is also required to explain our cross sections. It is impossible to quantify this without more specific information about the design of the storage elements within the processors. Nevertheless, it appears likely that enhanced charge collection mechanism is present in these devices. The nearly identical per bit cross sections that were measured for the IBM processor, with much smaller feature size, add further corroboration.

Finally, as noted by Dodd, et al. [18] and supported by modeling results in the device community [14,16], the track structure of ions is larger than the geometric size of critical regions within these highly scaled devices. This clearly affects charge collection, and will probably require a different metric than LET to define the sensitivity of highly scaled devices to upsets from heavy ions or proton recoils.

## VI. Conclusions

This paper presents the first results for high-performance commercial microprocessors that are fabricated with SOI processes. Even though the silicon film thickness is below 0.2 $\mu$m, the threshold LET values of the SOI processors are nearly the same as those of bulk/epi processors from the same manufacturers, indicating that little improvement in SEU sensitivity has resulted from the move to SOI technology. Results were nearly the same for both SOI processors, even though they have different feature sizes and core voltages.

Although the threshold LET did not change significantly, the cross sections of the SOI processors were about an order of magnitude lower than their bulk/epi counterparts, leading to a correspondingly lower upset rate in space environments. This shows that only modest improvement in SEU sensitivity can be expected as mainstream integrated circuits move to SOI technology. One SOI processor used a feature size of 0.13 $\mu$m, suggesting that this result may hold through at least one additional generation of device design.

The upset rates of these devices are low enough to allow their use in space applications where occasional upsets can be tolerated. Although a small number of "hangs" were observed during radiation tests, the cross section for this type of functional error is low enough so that "hangs are expected only occasionally, with an estimated rate of one in 25 years from galactic cosmic rays in deep space.

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